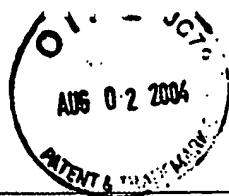


Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office					Atty. Docket No. IMPJ-0027A	Serial No.: Unassigned 10/813,907	
Information Disclosure Statement by Applicant (Use several sheets if necessary)					Applicant: Christopher J. Diorio et al. Filed: Herewith Group: Unassigned 3/30/04 2827		
U.S. Patent Documents							
Init.		Document No.	Date	Name	Class	Subclass	Filing Date
TP	A	5,761,121	6/2/1998	Chang	365	185.14	10/31/1996
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TP	O	Raszka, Jaroslav, et al., "Embedded Flash Memory for Security Applications in a 0.13µm CMOS Logic Process", IEEE 2004 International Solid-State Circuits Conference, February 16, 2004, pp. 46-47.					
Examiner	Trong Phan			Date Considered 12/17/05			
Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.							

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U.S. Patent Documents								
Init.		Document No.	Date	Name	Class	Subclass	Filing Date	
TP	P	2003/0206437	11/6/2003	Diorio et al.	365	185.03	7/9/2002	
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✓	T	2004/0052113	3/18/2004	Diorio et al.	365	185.21	9/16/2002	
Foreign Documents								
Translation								
Init.		Document No.	Date	Country	Class	Subclass	Yes	No
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)								
Examiner <i>Trong Phan</i>					Date Considered 12/17/05			
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Form PTO 1449 (Rev. 2-32)	U.S. Department of Commerce Patent and Trademark Office	FEB 10 2005 U.S. PATENT & TRADEMARK OFFICE	Atty. Docket No. IMPJ-0027A	Serial No. 10/813,907
Information Disclosure Statement by Applicant			Applicant: Christopher J. Diorio et al.	
(Use several sheets if necessary)			Filed: March 30, 2004	Group: 2818 2827

U.S. Patent Documents

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Translation

Init. Document No. Date Country Class Subclass Yes No

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TP	L	International Search Report, Application No.: PCT/US 03/31792, date of mailing August 12, 2004.
TP	M	Witters, et al., "Analysis and Modeling of On-Chip High-Voltage Generator Circuits for Use in EEPROM Circuits", IEEE Journal of Solid-State Circuits, VOL. 24, No. 5, October 1989, pp. 1372-1380.

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